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ABSTRACT:

THE DATE - 11/1/62 - A water-locked package and a device for removal of same. The package is a rectangular box with a water-tight lid. The lid is hinged to the box and is provided with a locking mechanism. The locking mechanism is a combination of a lock and a key. The lock is a cylindrical lock with a keyhole. The key is a cylindrical key with a notched end. The notched end of the key is inserted into the keyhole of the lock. The key is then turned, which causes the lock to rotate and the lid to open. The package is designed to be used for the transport of hazardous materials. The package is made of a material that is resistant to fire and explosion. The package is also designed to be easy to handle and to be safe to use.

terminal 11, at least one additional terminal 11
provided in the
central region 11, at least one terminal member 12;
17; 22; 23, and a
lateral member 14; 15, 16. A first end of the
reflected member 11
is connected to one of the first and second terminals 12A and 12B
and a second end of the
reflected member 11 is extended to a region 13
offset from the first
terminals 12, 12A, 12B. The terminal member 12; 17; 22;
23 is provided in
an outer region 13 of the semiconductor chip 10 with
terminal region 13,
and the second end of the reflected member 11 is
connected to the terminal
member 12; 17; 22; 23. CLAIMS

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to a wafer-level package, a method of manufacturing thereof, and a method of manufacturing semiconductor devices from such a wafer-level package. The present invention particularly relates to an improved wafer-level package to be tested by a preliminary test (PT) and a final test (FT), a method of manufacturing the wafer-level package, and a method of manufacturing semiconductor devices using such a wafer-level package.

[0002] Recently there is a need for more efficient manufacturing and testing processes of semiconductor devices. In order to achieve this, a full test (including PT and FT) is implemented on an uncut semiconductor wafer before being cut into individual semiconductor devices. As will be described below, the full test has several advantages over the related art in which the semiconductor wafer is cut into individual semiconductor devices and each of the semiconductor devices are tested individually.

[0003] The advantages include good handling efficiency, a possibility of sharing certain equipment and reduced space. If the wafer sizes are equal, handling equipment can be shared. Also, it is possible to save space otherwise taken up as a storage area and/or an installation area when accommodating individualized semiconductor devices (LSI chips) in containers such as a tray.

[0004] For higher density mounting, there is an increasing need for a KGD (Known-Good Die) and a real-chip-size package (a package having the same size as that of the semiconductor chip). However, with the package structure of the semiconductor device of the related art, which does not correspond to the KGD or the real-chip-size package, the area of the package is greater than that of the semiconductor chip. Therefore, the semiconductor wafer must be individualized at some point before packaging. Thus, with the package structure of the related art, the entire process, that is to say, from a manufacture process to a test process, cannot be implemented on the semiconductor wafer.

[0005] However, with the KGD or the real-chip-size package, since the final package configuration corresponds to the area of the semiconductor chip, the entire process can be implemented on the semiconductor wafer. Therefore, the above-described advantages can be obtained.

2. Description of the Related Art

[0006] Recently there is an increasing interest in a wafer-level package which is a package structure with which the entire process from the manufacturing process

to the testing process can be implemented on a semiconductor wafer. The wafer-level package includes a semiconductor wafer provided with a plurality of semiconductor chip circuits with chip terminals, external connection terminals, redistribution traces connecting the chip terminals and the external connection terminals, and an insulating material such as a sealing resin. The insulating material is provided for protecting the semiconductor chip circuits and the redistribution traces. A structure without the insulating material is also possible.

[0007] The wafer-level package may be used in two different configurations. One is in the form of a wafer (i.e., before being cut) and the other is in form of individual semiconductor devices (i.e., after cutting into individual semiconductor chip circuits).

[0008] In the following, the wafer-level package of the above-described structure will be described with regard to a test process thereof. With the wafer-level package, like that of the semiconductor devices of other configurations, the manufacture process includes a test process. The test process generally includes a preliminary test (PT) and a final test (FT).

[0009] The PT is a test implemented before providing the insulating material. The PT is a general test such as a conduction test of the interconnections, and thus does not include the operation test of the semiconductor chip circuit itself. Since the PT is implemented before providing the insulating material, the PT can be implemented using the chip terminals provided on the semiconductor chip circuit.

[0010] The PT is particularly advantageous for the package structure of the semiconductor devices of the related art (hereinafter, referred to as a conventional package), which are not designed for the KGD or for the real-chip-size package. In a manufacture process of the conventional package, the FT is followed by a cutting process (i.e., dicing process) for individualizing the semiconductor wafer into the semiconductor devices. Then, only those semiconductor devices which were determined good in the PT, are provided with the insulating material and undergo the FT. In other words, those semiconductor devices, which were determined bad in the PT, are not provided with the insulating material and also do not undergo the FT. Thus, the manufacture efficiency can be improved.

[0011] The FT is implemented after providing the insulating material. The FT is a total test including the operation test of the semiconductor chip circuit. Since the FT is implemented after the insulating material has been provided, the FT can only be implemented using the external connection terminals exposed from the insulating material. In other words, the terminals (such as the chip terminals) other than those generally used by the users are not exposed. Therefore, the chip terminals sealed in the insulating material cannot be used in the FT.

[0012] Therefore, in the related art, the wafer-level package is tested by, first, implementing the PT before

providing the insulating material using the chip terminals which are not yet covered with the insulating material. After the PT, the insulating material is provided, and then the FT is implemented using the external connection terminals exposed from the insulating material.

[0013] In the test process of the related art, the object of implementing the FT is to improve manufacture efficiency by avoiding the insulating material being provided on bad semiconductor devices and thus avoiding the FT being implemented thereon. On the contrary, with the wafer-level package, all semiconductor chip circuits, including circuits of the bad semiconductor devices, are provided with the insulating material and undergo the FT, so that it is not necessary to implement the PT before the FT.

[0014] Also, as has been described above, the wafer-level package is used for simplifying the manufacture process by using the semiconductor wafer from the manufacture process to the test process. For further simplifying the manufacture process, the PT and the FT, which in the related art were implemented as two separate tests, can be integrated into a single test process.

[0015] When the PT and the FT are integrated into a single test process, the integrated test process can be carried out either before providing the insulating material (i.e., when the PT is implemented in the related art) or after providing the insulating material (i.e., when the FT is implemented in the related art). When the integrated test process is implemented before providing the insulating material, it is not possible to detect any failure produced in the semiconductor chip circuit while providing the insulating material. Thus, the test process should be implemented in a later step in the manufacture process of the semiconductor device.

[0016] On the contrary, when the integrated test process is implemented after providing the insulating material, only the external connection terminals exposed from the insulating material may be connected to test equipment (e.g., a semiconductor tester). That is to say, the chip terminals include terminals which do not serve as the external connection terminals, but can be used for testing the semiconductor chip circuit (hereinafter referred to as test chip terminals). There is a drawback that the test chip terminals will be covered with the insulating material, so that the test using the test chip terminals cannot be implemented after providing the insulating material.

[0017] In order to avoid such a drawback, test terminals may be provided in a region of the semiconductor chip circuit region, which terminals are exposed from the insulating material and are connected to the above-described test chip terminals. Thus, with such test terminals, all tests including the PT and the FT (full test) can be implemented after providing the insulating material.

[0018] However, the test terminals will not be used after the test process, and thus become unwanted terminals for the package. Such test terminals provided on the semiconductor chip circuit forming region results in

an increase in the size of the semiconductor chip circuit forming region due to an area occupied by the test terminals. Accordingly, it is not possible to meet the requirement for a miniaturization of the semiconductor device.

[0019] Also, when the test terminals are provided at a position adjacent to the external connection terminals used for operating the semiconductor chip, the test terminals may also be mistakenly mounted on a mounting board. In such a case, a false operation may occur. Therefore, the test terminals should not remain on the package after the insulating material has been provided. [0020] Further, the PT can be omitted (that is to say, all tests can be implemented in the FT), but as has been described above, not all test chip terminals can be used in the FT. Therefore, tests, which used to be implemented in the PT only, cannot be implemented. For example, if the RAM and logic circuits are mounted in a mixed manner, a single test of the RAM cannot be carried out. At the same time, recently, since a high reliability is required for the semiconductor device, the PT cannot be omitted just for the sake of simplifying the manufacturing process.

[0021] From the above-described reasons, the PT and the FT have not been integrated in the related art. First, the PT is implemented, and then the insulating material is provided. Finally, the FT is implemented. Therefore, there is a problem that the manufacture process of the wafer-level package is complicated and thus the manufacture efficiency is decreased and the manufacture cost is increased.

SUMMARY OF THE INVENTION

[0022] Accordingly, it is a general object of the present invention to provide a wafer-level package, a method of manufacturing thereof, and a method of manufacturing a semiconductor device from such a wafer-level package which can solve the problems described above.

[0023] It is another and more specific object of the present invention to provide a wafer-level package, a method of manufacturing thereof, and a method of manufacturing a semiconductor device from such a wafer-level package which can improve a manufacturing efficiency and reduce a manufacturing cost.

[0024] In order to achieve the above objects according to the present invention, a wafer-level package includes

a semiconductor wafer having at least one semiconductor chip circuit forming region each including a semiconductor chip circuit and a plurality of chip terminals, the chip terminals including at least one test chip terminal and at least one non-test chip terminal;

at least one external connection terminal electrically connected to the at least one non-test chip terminal; at least one redistribution trace provided on the semiconductor wafer, a first end of the redistribution

trace being connected to one of the test chip terminals and a second end of the redistribution trace being extended out to a position offset from the one of the chip terminals

at least one testing member provided in an outer region of the semiconductor chip circuit forming region, the second end of the redistribution trace being connected to the least one testing member, and an insulating material covering at least the redistribution trace, the at least one external connection terminal and the at least one testing member being exposed from the insulating material

[0025] With the wafer-level package described above, even when the testing member is provided, the semiconductor chip circuit forming region will not become large. Therefore, the size of each individualized semiconductor device will be small compared to that of the structure in which the testing member is provided in the semiconductor chip circuit forming region.

[0026] Also, the testing member is provided in the outer region of the semiconductor chip circuit forming region, which outer region is to be removed upon individualizing into semiconductor devices. Therefore, even if the testing member is provided on the wafer-level package, the operating condition of the individualized semiconductor device will not be altered.

[0027] In order to achieve the above object, a wafer-level semiconductor device is disclosed, which includes

a semiconductor wafer having chip circuit forming regions

at least one testing member provided in an outer region of the chip circuit forming regions, and

a line provided on the semiconductor wafer and connecting the at least one testing member and a test terminal provided in one of the chip circuit forming regions

[0028] It is still another object of the present invention to provide an easier method of manufacturing the above-described wafer-level package.

[0029] In order to achieve the above object, a method of manufacturing a wafer-level package includes the steps of:

a) preparing a semiconductor wafer having at least one semiconductor chip circuit forming region each provided with a semiconductor chip circuit and a plurality of chip terminals, at least one of the chip terminals being a test chip terminal and at least one being a non-test chip terminal,

b) providing a redistribution layer including an insulating film having through holes on the semiconductor wafer and an electrically conductive film formed on the insulating film, the film being formed into redistribution traces having a predetermined pattern,

c) providing external connection terminals and at

least one testing member on the redistribution layer, the at least one testing member being provided at an outer region of the at least one semiconductor chip circuit forming region and connected to the test chip terminal via at least one of the redistribution traces,

d) testing the at least one semiconductor chip circuit using the at least one testing member, and

e) providing a sealing resin on the redistribution layer in such a manner that top parts of the external connection terminals and the at least one testing member are exposed from the sealing resin.

[0030] With the above-described method, the external connection terminals and the testing members can be provided simultaneously. Further, the PT and the ET can be implemented simultaneously. Thus, the package manufacturing process and the test process can be simplified.

[0031] It is yet another object of the present invention to provide an easier method of manufacturing at least one semiconductor device using the above-described wafer-level package.

[0032] In order to achieve the above-described object, a semiconductor device manufacturing method includes the steps of:

a) manufacturing the wafer-level package as described above,

b) testing the at least one semiconductor chip circuit provided in the at least one semiconductor chip circuit forming region by means of said at least one testing member, and

c) after the step b), cutting the wafer-level package along the outer region so as to manufacture at least one individualized semiconductor devices.

[0033] With the above-described method, external connection terminals and the testing member can be provided simultaneously. Further, the PT and the ET can be implemented simultaneously. Thus, the package manufacturing process and the test process can be simplified.

[0034] Also, the testing member will be removed when individualizing the semiconductor devices, so that the operating condition of the individualized semiconductor device will not be altered.

[0035] It is yet another object of the present invention to provide a semiconductor device which can be manufactured according to a method of the present invention.

[0036] In order to achieve the above object, a semiconductor device includes

a semiconductor chip,

a test terminal and a non-test terminal provided to the semiconductor chip, and

a line which is connected to the test terminal and extends out of a circuit forming region.

[0037] Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] Fig. 1 is a diagram showing a connection state of a wafer-level package of a first embodiment of the present invention

[0039] Fig. 2 is a partial sectional view showing the wafer-level package of the first embodiment of the present invention taken along a broken line I-I

[0040] Fig. 3 is a plan view showing the wafer-level package of the first embodiment of the present invention

[0041] Fig. 4 is a partial sectional view showing a wafer-level package of a second embodiment of the present invention

[0042] Fig. 5 is a diagram showing a connection state of a wafer-level package of a third embodiment of the present invention

[0043] Fig. 6 is a diagram showing a connection state of a wafer-level package of a fourth embodiment of the present invention

[0044] Fig. 7 is a diagram showing a connection state of a wafer-level package of a fifth embodiment of the present invention

[0045] Fig. 8 is a diagram showing a connection state of a wafer-level package of a sixth embodiment of the present invention

[0046] Fig. 9 is a diagram showing a connection state of a wafer-level package of a seventh embodiment of the present invention

[0047] Fig. 10 is a diagram showing a connection state of a wafer-level package of an eighth embodiment of the present invention

[0048] Fig. 11 is a diagram showing a connection state of a wafer-level package of a ninth embodiment of the present invention

[0049] Fig. 12 is a diagram showing a connection state of a wafer-level package of a tenth embodiment of the present invention

[0050] Fig. 13 is a plan view showing a wafer-level package of an eleventh embodiment of the present invention

[0051] Fig. 14 is a diagram showing a connection state of a wafer-level package of a twelfth embodiment of the present invention

[0052] Fig. 15 is a diagram showing a connection state of a wafer-level package of a thirteenth embodiment of the present invention

[0053] Fig. 16 is a flowchart showing a method of manufacturing a semiconductor device using a wafer-level package of one embodiment of the present invention

[0054] Figs. 17A to 17D are cross-sectional diagrams showing a package manufacture process of the method

of manufacturing a semiconductor device using a wafer-level package of one embodiment of the present invention

[0055] Fig. 18 is a cross-sectional diagram showing a test process of the method of manufacturing a semiconductor device using a wafer-level package of one embodiment of the present invention

[0056] Fig. 19 is a cross-sectional diagram showing a cutting process of the method of manufacturing a semiconductor device using a wafer-level package of one embodiment of the present invention

[0057] Fig. 20 is a partial sectional view showing a wafer-level package of a fourteenth embodiment of the present invention

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0058] In the following, principles and embodiments of the present invention will be described with reference to the accompanying drawings

[0059] Figs. 1 to 3 are diagrams showing a wafer-level package 10A of a first embodiment of the present invention. Fig. 1 is a diagram showing a connection state of the wafer-level package 10A, Fig. 2 is a diagram showing a connection state of the wafer-level package 10A and Fig. 3 is a diagram showing a connection state of the wafer-level package 10A

[0060] The wafer-level package 10A may be used as an uncut wafer or may be cut into individualized semiconductor devices 40 (shown in Fig. 19) having respective semiconductor chip circuits

[0061] As shown in Fig. 2, the wafer-level package 10A includes a semiconductor wafer 11 provided with external connection terminals 14, redistribution traces 15, test terminals 16, and an insulating layer 17 (insulating material)

[0062] The semiconductor wafer 11 is, for example, a silicon substrate provided with a plurality of semiconductor chip circuit forming regions 12 (hereinafter referred to as circuit regions). The circuit region 12 is provided with a semiconductor chip circuit and a plurality of chip terminals 13 formed thereon. The chip terminals 13 are connected to the semiconductor chip circuits. Thus, the semiconductor chip circuit will operate when signals and electrical power are supplied to the chip terminals 13

[0063] Also, the plurality of chip terminals 13 may be categorized into two groups according to their functions. A first group includes chip terminals directly contributing to the operation of the semiconductor chip circuit, and the other group includes chip terminals used only for testing the semiconductor chip circuit. In the following description, the chip terminals in the latter group (i.e., chip terminals used for testing the semiconductor chip circuit) will be referred to as test chip terminals 13A. The chip terminals other than the test chip terminals 13A will be referred to as non-test chip terminals 13B.

[0064] The external connection terminals 14 are terminals used for mounting the wafer-level package 10A or the individualized semiconductor devices 40 on a mounting board (not shown). In the present embodiment, the external connection terminals 14 are directly provided on the non-test chip terminals 13B and are not provided on the test chip terminals 13A. Therefore, in the present embodiment, the external connection terminals 14 are provided at positions corresponding to the non-test chip terminals 13B. The external connection terminals 14 are provided so as to protrude by a predetermined amount from the upper surface of the semiconductor wafer 11. The external connection terminals 14 may be provided by techniques such as sputtering deposition and metal plating.

[0065] The redistribution traces 15 are made of an electrically conductive layer and are formed into a predetermined pattern on the upper surface of the semiconductor wafer 11. One end of the redistribution trace 15 is connected to the chip terminal 13 (13A) while the other end of the redistribution trace 15 is connected to the test terminal 16. In the cross sectional diagram, the redistribution trace 15 seems to extend to the external connection terminal 14; however, as can be seen in Fig. 1, in fact, the external connection terminal 14 is not connected to the redistribution trace 15. Thus, by providing the redistribution traces 15 on the semiconductor wafer 11, the chip terminals 13 can be extended to desired positions on the semiconductor wafer 11. Then, the external connection terminals 14 or the test terminals 16 can be formed at the desired positions.

[0066] Thus, by providing the redistribution traces 15 there is greater freedom in the layout of the terminals. That is to say, with the redistribution traces 15, the respective terminals 13 can be pulled out to positions not only within the circuit region 12 but also outside the circuit region 12. Hereinafter, the region outside the circuit region 12 is referred to as an outer region 18.

[0067] In the present embodiment, as has been described above, the external connection terminals 14 are directly formed on the non-test chip terminals 13B. Therefore, the redistribution traces 15 extend only from the test chip terminals 13A. Also, though not shown, an insulating film is provided on the upper part of the circuit region 12, and the redistribution trace 15 is formed on the insulating film. Therefore, even if the redistribution traces 15 are formed on the circuit region 12, the redistribution traces 15 and the semiconductor chip circuit will not be short-circuited.

[0068] The test terminals 16 are used for testing the semiconductor chip circuit formed in the circuit region 12. The test terminals 16 are provided so as to protrude by a predetermined amount from the upper surface of the semiconductor wafer 11. In a similar manner to the external connection terminals 14, the test terminals 16 may be provided by techniques such as sputtering, deposition and metal plating.

[0069] Also, as shown in Fig. 2, the test terminals 16

are configured such that the height of the protrusions and shapes thereof are equal to those of the external connection terminals 14. The test terminals 16 are, via the above-described redistribution traces 15, connected to the test chip terminals 13A provided in the circuit region 12. Therefore, the test terminals 16 are terminals only used for testing the wafer-level package 10A.

[0070] The insulating layer 17 is made of an insulating material, e.g., SiO_2 , having a predetermined thickness. The insulating layer 17 protects the semiconductor chip circuit provided in the circuit region 12, the chip terminals 13, and the redistribution traces 15. In the present embodiment, the insulating layer 17 is provided on the entire surface of the semiconductor wafer 11, with the above-described external connection terminals 14 and the test terminals 16 being exposed (or protruded) from the insulating layer 17.

[0071] Therefore, even after providing the insulating layer 17 on the semiconductor wafer 11, an electrical conduction with the semiconductor chip circuit can be achieved by means of the external connection terminals 14 and the test terminals 16.

[0072] Now, the position of the test terminals 16 of the wafer-level package 10A of the above-described structure will be described. As has been described above, the test terminals 16 are connected to the test chip terminals 13A via the redistribution traces 15. Also, the redistribution traces 15 can be extended to positions not only within the circuit region 12 but also to the outer region 18.

[0073] The present embodiment is characterized in that the redistribution traces 15 are extended out of the circuit region 12 to the outer region 18, and the test terminals 16 are provided in the outer region 18. Also, when the wafer-level package 10A is used as individualized semiconductor devices 40, a cutting (scribing) process is implemented on the wafer-level package 10A. The test terminals 16 are provided on the positions to be scribed (i.e., scribe regions). In Fig. 3, the scribe regions are indicated by dash-dot lines.

[0074] With the wafer-level package 10A of the present embodiment, each of the test chip terminals 13A is extended out of the circuit region 12 to the outer region 18 by means of the redistribution trace 15. Then, at an end extended out in the outer region 18, the redistribution trace 15 is provided with the test terminal 16 exposed from the insulating layer 17. Thus, the test terminals 16 can be used even after the insulating layer 17 has been provided.

[0075] Thus, since the test can be implemented using both the external connection terminals 14 and the test terminals 16, the PT, which was implemented before providing the insulating layer 17, and the ET, which was implemented after providing the insulating layer 17, can now be implemented simultaneously. Accordingly, with a simultaneous full test, the test process (manufacture process) can be simplified and the manufacturing cost can be reduced.

[0076] Also, by providing the redistribution traces 15, the test terminals 16 are provided in the outer region 18 (outside the circuit region 12). Thus, the area of the circuit region 12 will not increase even if the test terminals 16 are provided. Therefore, the size of the individualized semiconductor device 40 can be reduced.

[0077] Further, the outer region 18, in which the test terminals 16 are provided, is a region to be removed upon individualizing the wafer-level package 10A into the semiconductor devices 40. Therefore, when the semiconductor devices 40 are individualized, the test terminals 16 will be removed together with the outer region 18, and will not remain on the semiconductor device 40. Therefore, even if the test terminals 16 are provided on the wafer-level package 10A, the operating condition of the individualized semiconductor device 40 will not be altered.

[0078] Also, in the above-described embodiment, the test terminals 16 are provided in the scribe regions (see Fig. 3). However, the test terminals 16 can be provided at positions not only within the scribe regions, but also in other regions in the outer region 18 other than the scribe regions (e.g., peripheral positions of the semiconductor wafer 11).

[0079] In the following, a second embodiment of the present invention will be described.

[0080] Fig. 4 is a partial sectional view showing a wafer-level package 10B of a second embodiment of the present invention. In Fig. 4, components which are the same as those of the wafer-level package 10A of the first embodiment illustrated in Figs. 1 to 3 are indicated with the same reference numbers, and detailed explanations thereof are omitted. This also applies to each of the embodiments described with reference to Figs. 5 to 20.

[0081] In the wafer-level package 10B of the second embodiment, the semiconductor wafer 11 is provided with a redistribution layer 19. The redistribution layer 19 is provided with the external connection terminals 14, the test terminals 16 and a sealing resin 22 (insulating material).

[0082] The redistribution layer 19 includes the redistribution traces 15, an insulating film 20, and through holes 21. The insulating film 20 is made of an insulating material, e.g., SiO_2 , and is provided with the redistribution traces 15 having a predetermined pattern. Also, the insulating film 20 is provided with the through holes 21. The chip terminals 13 provided in the circuit region 12 and the redistribution traces 15 are electrically connected by means of the through holes 21.

[0083] The sealing resin 22 may be an epoxy-type resin, and can be provided on the entire surface of the semiconductor wafer 11, for example, by molding. Also, the above-described external connection terminals 14 and the test terminals 16 penetrate through this sealing resin 22 and protrude upwards, so as to enable an electrical connection with an external part. Also, the external connection terminals 14 are connected to the chip ter-

minals 13 provided in the circuit region 12 by means of through holes 21, but such structure is not shown in the figure for the sake of clarity.

[0084] The wafer-level package 10B of the above structure may also achieve the same effect as that of the wafer-level package 10A of the first embodiment. Further, in the present embodiment, the sealing resin 22 is made of an epoxy-type resin, which is commonly used as the resin package material. Therefore, the semiconductor wafer 11 (the semiconductor chip circuit, the redistribution traces 15, etc.) is securely protected, thus improving the reliability of the wafer-level package 10B. Also, the sealing resin 22 need not be made of the epoxy-type resin, but can also be made of other resin such as polyimide.

[0085] In the following, a third embodiment of the present invention will be described.

[0086] Fig. 5 is a diagram showing a connection state of a wafer-level package 10C of a third embodiment of the present invention. The wafer-level package 10A of the first embodiment described with reference to Figs. 1 to 3 relates to a structure in which the external connection terminals 14 are formed directly on the non-test chip terminals 13B. On the contrary, the present embodiment is characterized in that it is provided with internal redistribution traces 23 inside the circuit region 12, so that the non-test chip terminals 13B and the external connection terminals 14 are provided at mutually offset positions.

[0087] Thus, the positions of the external connection terminals 14 do not necessarily correspond with the positions of the non-test chip terminals 13B. Also, because the non-test chip terminals 13B and the external connection terminals 14 are provided at mutually offset positions, the circuit structure of the semiconductor chip circuit within the circuit region 12 can be designed with greater freedom.

[0088] In the following, a fourth embodiment of the present invention will be described.

[0089] Fig. 6 is a diagram showing a connection state of a wafer-level package 10D of a fourth embodiment of the present invention. The wafer-level package 10D of the present embodiment is characterized in that a fuse 24 is provided at an intermediate position of one of the redistribution traces 15 extends out to the outer region 18. The fuse 24 prevents an excessive power supply between the test chip terminal 13A and the test terminal 16. One of the test chip terminals 13A is a power supply terminal, and the test terminals 16 are connected to a power supply line 42.

[0090] For example, when implementing a burn-in test on a wafer-level package, it is often difficult to provide a power supply line independently to each semiconductor chip circuit. As in the present embodiment, by sharing the power supply line 42 between the plurality of semiconductor chip circuits, the burn-in test can be implemented at a reduced cost.

[0091] However, when sharing the power supply line

42 between the plurality of semiconductor chip circuits. If a semiconductor chip circuit has bad DC characteristics (power supply short circuit), there is a risk of burning other semiconductor chip circuits. By providing the fuse 24, even if an excessive power supply occurs due to the presence of a bad semiconductor chip circuit, the fuse 24 will break so that other normal semiconductor chip circuits will be prevented from being damaged.

[0092] Further, the fuse 24 will not remain on the semiconductor device 40 since the fuse 24 is provided in the outer region 18, and thus is removed when individualizing into semiconductor devices 40. Therefore, even if the fuse 24 is provided, the operating condition of the individualized semiconductor device 40 will not be altered.

[0093] In the following, a fifth embodiment of the present invention will be described.

[0094] Fig. 7 is a diagram showing a connection state of a wafer-level package 10E of a fifth embodiment of the present invention. The wafer-level package 10E of the present embodiment is characterized in that the test terminals 16 provided for respective ones of the plurality of circuit regions 12 are connected by a common line 25 formed in the external area 18.

[0095] With this structure, by supplying test signals to one of the test terminals 16, the test signals can be simultaneously supplied to the plurality of test terminals 16 via the common line 25. Therefore, a number of interconnections can be reduced. Also, test efficiency is improved compared to a structure in which respective signals are provided to each one of the test terminals 16.

[0096] Also, the common line 25 is provided in the outer region 18, and thus is removed when individualizing into semiconductor devices 40. Therefore, even if the common line 25 is provided on the wafer-level package 10E, the operating condition of the individualized semiconductor device 40 will not be altered.

[0097] In the following, a sixth embodiment of the present invention will be described.

[0098] Fig. 8 is a diagram showing a connection state of a wafer-level package 10F of a sixth embodiment of the present invention. The wafer-level package 10F of the present embodiment is characterized in that the non-test chip terminals 13B of the plurality of the semiconductor chip circuits provided on the semiconductor wafer 11 are connected by joining lines 26. In detail, in the embodiment shown in Fig. 8, the chip terminal 13C provided in the circuit region 12A and the chip terminal 13D provided in the circuit region 12B are connected by the joining line 26.

[0099] Some of the non-test chip terminals 13B will be used to improve the test efficiency and reduce the number of interconnections, so that such non-test chip terminals 13B may remain connected during the test. Thus, by connecting such non-test chip terminals 13B (13C, 13D) by the joining line 26, it is possible to improve the test efficiency and reduce the number of interconnections.

[0100] Also, the joining lines 26 are provided in the outer region 18, and thus are removed when individualizing into semiconductor devices 40. Therefore, even if the joining lines 26 are provided on the wafer-level package 10F, the operating condition of the individualized semiconductor device 40 will not be altered.

[0101] In the following, a seventh embodiment of the present invention will be described.

[0102] Fig. 9 is a diagram showing a connection state of a wafer-level package 10G of a seventh embodiment of the present invention. The wafer-level package 10G of the present embodiment is characterized in that the common lines 25 are provided in the outer region 18, and the redistribution traces 15 are connected to these common lines 25. Also, a test pad 27 is provided at a part of the common line 25. The test pad 27 is provided so as to be exposed from the insulating layer 17 (or sealing resin 22).

[0103] With the structure described above, the plurality of redistribution traces 15 corresponding to the plurality of circuit regions 12 are connected via the common lines 25. Thus, by supplying test signals to the test pads 27, the test signals can be simultaneously supplied to the plurality of semiconductor chip circuits via the common line 25. Therefore, a number of interconnections can be reduced. Also, since there is no need to provide the test terminal 16 for each of the semiconductor chip terminals, it is possible to simplify the structure and the manufacturing processes of the wafer-level package 10G.

[0104] In the following, an eighth embodiment of the present invention will be described.

[0105] Fig. 10 is a diagram showing a connection state of a wafer-level package 10H of an eighth embodiment of the present invention. The wafer-level package 10H of the present embodiment is characterized in that a plurality of units 28, 29 having different functions are provided in the circuit region 12. Also, the redistribution traces 15 are extended out from each one or a combination of the plurality of units 28, 29 to the outer region 18. On the end positioned in the outer region 18, the redistribution trace 15 is provided with the test terminal 16.

[0106] In detail, in the present embodiment, the circuit region 12 is provided with a logic part (LOGIC) 28 and a random access memory part (RAM) 29. The LOGIC 28 and the RAM 29 are connected by internal connections 30. Also, the LOGIC 28 is provided with chip terminals (not shown) having the external connection terminals 14 connected thereto. The semiconductor device having a mixed structure of units with different properties or functions, such as the RAM and the LOGIC, is referred to as a system LSI device. Recently, as a result of a higher density and higher performance of the semiconductor devices, more system LSI devices are used. However, it is difficult to individually test the units provided in the system LSI device.

[0107] This is because these units are interconnected

by the internal connections 30 in the same circuit region 12 so that there may be a unit that cannot be directly accessed by the external connection terminals 14. For example, with the structure of the present embodiment, the LOGIC 28 and the RAM 29 are connected via the internal connections 30, and the external connection terminals 14 serve as access terminals to the LOGIC 28. Thus, the RAM 29 cannot be directly accessed via the external connection terminals 14.

[0108] Now, the function of the system LSI device will be described as a whole. The LOGIC 28 accesses the RAM 29 via the internal connections 30 so as to acquire and process data in the RAM 29. Then, the thus-obtained data is output from the external connection terminals 14. Therefore, with the system LSI of the structure of the related art, it is not possible to directly access the RAM 29. In other words, the RAM 29 cannot be tested individually in the related art.

[0109] However, with the structure of the present embodiment, it is now possible to test the RAM 29 individually. The redistribution traces 15 are pulled out to the outer region 18 from the RAM 29, and the test terminals 16 are provided on the redistribution trace 15. Thus, the RAM 29, which is a unit that is not directly connected to the external connection terminals 14, can be tested.

[0110] Accordingly, since it is now possible to test the RAM 29, the reliability of the test can be improved. Also, the redistribution traces 15 and the test terminals 16 will be removed when cutting the wafer-level package 10H into individualized semiconductor devices 40. Therefore, the operating condition of the individualized semiconductor device 40 will not be altered.

[0111] In the following, a ninth embodiment of the present invention will be described.

[0112] Fig. 11 is a diagram showing a connection state of a wafer-level package 10I of a ninth embodiment of the present invention. The wafer-level package 10I of the present embodiment includes a burn-in test circuit 32 (Built-In Self Test: BIST). The redistribution traces 15 are extended out from the BIST 32 to the outer region 18. The test terminals 16 are provided on the redistribution traces 15 in the outer region 18.

[0113] The BIST 32 implements the test on a main circuit part 31, so that it is possible to read out only the result of the test from the test chip terminals 13A. However, the test chip terminals 13A serving as input/output terminals of the BIST 32 are used only in the PT (or cannot not be used in the FT), since the test chip terminals 13A cannot be left as the external connection terminals after wafer packaging.

[0114] On the contrary with the present embodiment, the test chip terminals 13A, serving as the input/output terminals of the BIST 32 after wafer packaging, can be accessed via the test terminals 16 and the redistribution traces 15. Thus, a test using the BIST 32 can be implemented in the FT. Thus, the PT will be not as necessary as it used to be, so that the test (full test) can be implemented only with the FT and without the PT.

[0115] In the following, a tenth embodiment of the present invention will be described.

[0116] Fig. 12 is a diagram showing a connection state of a wafer-level package 10J of a tenth embodiment of the present invention. The wafer-level package 10J of the present embodiment is characterized in that a circuit exclusively used for a burn-in test 32A (herein after referred to as a BI circuit 32A) is provided in the outer region 18.

[0117] In detail, the redistribution trace 15 is provided from the test chip terminal 13A in the circuit region 12 to the outer region 18. The redistribution trace 15 is connected to the BI circuit 32A. As has been described above, the BI circuit 32A and the redistribution trace 15 are provided in the outer region 18. Also, the test terminal 16 may be provided directly on the BI circuit 32A.

[0118] Now, a full test on the wafer-level package and the normal wafer (here, the wafer-level package and the normal wafer will be referred to as a wafer) will be described. In the related art, the full test on the wafer was not often implemented before individualizing the wafer into the semiconductor devices. One of the reasons is that it is difficult to implement a burn-in test on the uncut semiconductor wafer. In other words, with the currently available contactor, it is difficult to contact all of the plurality of terminals (external connection terminals 14 and the test terminals 16) provided on each of the semiconductor chip terminals provided on the wafer. This is also because there are several tens of thousands of terminals provided on the wafer and thus the terminal pitch is narrow.

[0119] In order to minimize such a problem, an attempt has been made to incorporate the BI circuit 32A into the circuit region 12, and then contacting a few terminals (burn-in terminals accessing the burn-in circuit). However, with the wafer-level package of the related art in which the BI circuit 32A is incorporated within the circuit region 12, the burn-in terminals will, together with the external connection terminals 14, remain in the semiconductor device 40, thus producing the same problem as above.

[0120] However, with the structure of the present embodiment, the redistribution traces 15 are pulled out from the BI circuit 32A to the outer region 18. The test terminals 16 serving as the burn-in terminals are provided on the redistribution traces 15 in the outer region 18 so that it is possible to access the BI circuit 32A via the test terminals 16. Thus, the BI circuit 32A can be used after providing the insulating layer 17 (sealing resin 22).

[0121] Accordingly, it is possible to implement a burn-in test on the wafer-level package 10J so that a test with an increased reliability is possible. Also, since the test terminals 16 will be removed when individualizing into the semiconductor devices 40, the operating condition of the individualized semiconductor device 40 will not be altered.

[0122] In the following, an eleventh embodiment of the present invention will be described.

[0123] Fig. 13 is a plan view showing a wafer level package 10K of an eleventh embodiment of the present invention. The wafer-level package 10K of the present embodiment is characterized in that a test history recording part 33 (test history storage) is provided in the outer region 18 on the semiconductor wafer 11.

[0124] The test history recording part 33 is connected to all semiconductor chip circuits on the semiconductor wafer 11 via redistribution traces 35 exclusively used for recording provided in the outer region 18. Also, the test history recording part 33 is provided with access terminals 34 (input/output terminals).

[0125] The access terminals 34 protrude upwards from the insulating layer 17 (sealing resin 22) formed on the semiconductor wafer 11, so that it is possible to access the test history recording part 33 after providing the insulating layer 17 (sealing resin 22). By accessing the test history recording part 33, it is possible to store/retrieve the test data such as test history and the positions of the bad semiconductor chip circuits.

[0126] With the wafer-level package 10K provided with the insulating layer 17 or the sealing resin 22, the whole semiconductor wafer 11 is covered with the resin (in many cases a black resin). Thus, it is difficult to implement a visual inspection. Also, since the semiconductor chip circuits are provided on the semiconductor wafer 11 with a high density, it is difficult to imprint characters or codes indicating a vast amount of test history information on the peripheral part of the wafer-level package 10K.

[0127] However, with the test history recording part 33, a vast amount of test history information of the wafer-level package 10K can be easily written in/read out. Thus, efficiency and accuracy of the test can be improved. Also, since the test history recording part 33 is provided on the outer region 18, it will be removed when individualizing into the semiconductor devices 40. Thus, the operating condition of the individualized semiconductor device 40 will not be altered.

[0128] In the following, a twelfth embodiment of the present invention will be described.

[0129] Fig. 14 is a diagram showing a connection state of a wafer-level package 10L of a twelfth embodiment of the present invention. The wafer-level package 10L of the present embodiment is provided with a test support element 36 for testing the semiconductor chip circuit on the outer region 18 on the semiconductor wafer 11. Also, the redistribution traces 15 connected to the test chip elements 13A provided in the circuit region 12 are connected to the test support element 36 via the common line 25.

[0130] The test support element 36 may be an electronic element such as a test LSI circuit or a resistance. With the test support element 36, the efficiency of the wafer-level test can be improved. Also, it is advantageous when implementing a high-frequency test, since the distance between the test chip terminal 13A and the test support element 36 can be shortened.

[0131] Also, since the test support element 36 and the common line 25 are provided in the outer region 18, they will be removed when individualizing into the semiconductor devices 40. Thus, the operating condition of the individualized semiconductor device 40 will not be altered.

[0132] In the following, a thirteenth embodiment of the present invention will be described.

[0133] Fig. 15 is a diagram showing a connection state of a wafer-level package 10M of a thirteenth embodiment of the present invention. The wafer-level package 10M of the present embodiment is characterized in that the test terminals 16 and dummy terminals 38 are provided in an identification area 37 with a predetermined rule, thus enabling an identification.

[0134] The identification area 37 is provided in the outer region 18 of the semiconductor wafer 11, and the test terminals 16 are connected to the corresponding circuit region 12 by means of the redistribution traces 15. Also, the dummy terminal 38 is not connected to the redistribution trace 15, but has the same shape as that of the test terminal 16 and is exposed from the insulating layer 17 (sealing resin 22).

[0135] As has been described above, it is difficult to visually inspect the wafer-level package 10K provided with the insulating layer 17 or the sealing resin 22. However, the test terminals 16 and the dummy terminals 38 are arranged with a predetermined rule indicating the characteristics (e.g., indexmark, type code, lot identification) of the semiconductor wafer 11 and are exposed from the insulating layer 17 (sealing resin 22). Therefore, the semiconductor wafer 11 can be identified by viewing the positions of the test terminals 16 and the dummy terminals 38, so that the identification process can be implemented on the wafer-level package 10M, which is not particularly suitable for visual inspection.

[0136] Further, the test terminals 16 and the dummy terminals 38 having the identification function are also removed when individualizing into the semiconductor devices 40. Therefore, the operating condition of the individualized semiconductor device 40 will not be altered. Also, if the identification is possible by viewing the positioning of the test terminals 16, it is not always necessary to provide the dummy terminals 38.

[0137] In the following, a fourteenth embodiment of the present invention will be described.

[0138] Fig. 16 is a cross-sectional view showing a wafer-level package 10N of a fourteenth embodiment of the present invention. In wafer-level packages 10A to 10M, there is provided the insulating layer 17 or the sealing resin 22 on the redistribution trace 15, whereas the wafer-level package 10N is not provided with the insulating material (insulating layer 17, sealing resin 22, etc.). Note that an insulating film is provided between the semiconductor chip circuit and the redistribution traces 15.

[0139] With the above-described structure, the redistribution traces 15 are always exposed outside, so that the test terminals 16 can be formed on the redistribution

traces 15 exposed from the circuit 12. Thus, each of the semiconductor chip circuits can be tested after the wafer-level package 10N has been manufactured.

[0140] However, as has been described, it is preferable that terminals not used by the users are not provided in the circuit region 12. Thus, instead of the test terminals 16, flat connection pads capable of being connected to test contacts 41 can be provided in the circuit region 12 (see Fig. 18). However, in order to achieve a proper connection with the test contact, the connection pad must have a certain area. Then, with this structure, the area of the circuit region 12 will become too large.

[0141] On the contrary, with the wafer-level package 10N of the present embodiment, the chip terminal 13 used during the test is extended out to the position outside the circuit region 12 by means of the redistribution trace 15, while providing the test terminal 16 on the redistribution traces 15 thus extended out. Therefore, the circuit region 12 will not become too large even if the test terminals 16 are provided. Therefore, compared to the structure where the test terminals are provided in the circuit region 12, the circuit region 12 can be used efficiently, and thus when individualized, each of the semiconductor device 40 will become compact.

[0142] Also, the test terminals 16 are provided at positions to be removed upon individualizing into semiconductor devices 40 so that the test terminals 16 will not remain on the individualized semiconductor devices 40. Therefore, even if the test terminals 16 are provided on the wafer-level package 10N, the operating condition of the individualized semiconductor device 40 will not be altered.

[0143] In the following, a method of manufacturing the semiconductor device (hereinafter referred to as a semiconductor device manufacturing method) using the wafer-level package of an embodiment of the present invention will be described.

[0144] The semiconductor device manufacturing method will be described with reference to Figs. 16 to 19. Fig. 16 is a flowchart showing the semiconductor device manufacturing method and Figs. 17A to 19 are detailed diagrams showing the semiconductor device manufacturing method.

[0145] As shown in Fig. 16, the semiconductor device manufacturing method of the present embodiment includes a package manufacturing process (step 1), a test process (step 2) and a cutting process (step 3).

[0146] In the package manufacturing process (step 1), the wafer-level package 10B of the second embodiment shown in Fig. 4 is manufactured. In the test process (step 2), the semiconductor chip circuits provided on the wafer-level package 10B are tested by means of the test terminals 16 and the external connection terminals 14. In the cutting process (step 3), the outer region 18 (scribe regions) of the wafer-level package 10B is cut so as to manufacture the individualized semiconductor devices 40. In the following, each of the processes will be described in detail.

[0147] Figs. 17A to 17D are diagrams showing the package manufacturing process (step 1) for manufacturing the wafer-level package 10B. In order to manufacture the wafer-level package 10B, first, as shown in Fig. 17A, the semiconductor wafer 11 provided with the circuit regions 12 is prepared.

[0148] Then, as shown in Fig. 17B, the insulating film 20 (SiO₂ film) having a predetermined thickness is provided on the semiconductor wafer 11. Also, using a photolithography technique, small holes are formed in the insulating film 20. Then, an electrically conductive film is formed on the insulating film 20 by plating (or by other thin-film forming techniques such as sputtering and deposition). Further, the redistribution traces 15 having a predetermined pattern are formed by etching.

[0149] When providing the electrically conductive material, some of the electrically conductive material will be introduced into the above-described small holes, so that the through holes 21 are formed. Also, the lower ends of the through holes 21 are electrically connected to the chip terminals 13 (13A) provided in the circuit region, and the upper ends are electrically connected to the redistribution traces 15. Thus, the redistribution layer 19 is formed on the semiconductor wafer 11.

[0150] Then, after providing the redistribution layer 19 as described above, the external connection terminals 14 and the test terminals 16 are formed as shown in Fig. 17C. As has been described above, the external connection terminals 14 and the test terminals 16 may be formed simultaneously because their shapes are identical. Therefore, the present embodiment is described regarding to a case in which the external connection terminals 14 and the test terminals 16 are formed simultaneously.

[0151] In detail, a mask having openings at positions corresponding to the external connection terminals 14 and the test terminals 16 is used, and the external connection terminals 14 and the test terminals 16 are grown by plating (or sputtering or deposition). The heights of the terminals 14, 16 may be adjusted by controlling the plating time. Thus, in the present embodiment, since the external connection terminals 14 and the test terminals 16 are formed simultaneously, the manufacturing process can be simplified compared to a structure in which the terminals 14, 16 are formed in separate steps.

[0152] In the present embodiment, the external connection terminals 14 are formed directly on the chip terminals 13B provided on the semiconductor chip circuit, and the test terminals 16 are formed on the redistribution traces 15. Also, the test terminals 16 are formed at the position outside the circuit area 12, i.e., in the outer region 18.

[0153] After the external connection terminals 14 and the test terminals 16 are formed in the manner described above, the semiconductor wafer 11 is mounted on the mold (not shown) and the resin mold process is implemented. Thus, as shown in Fig. 17D, the sealing resin 22 is formed on the semiconductor wafer 11. As has

been described above, the sealing resin 22 may be made of an epoxy-type resin.

[0154] When forming the sealing resin 22, a molding process is implemented so that the predetermined top part of the external connection terminals 14 and the test terminals 16 are exposed from the sealing resin 22. Therefore, even after the sealing resin 22 (insulating material) has been provided, the semiconductor chip circuit is accessible via the external connection terminals 14 and the test terminals 16.

[0155] Thus, by implementing the above-described processes, the wafer-level package 10B is manufactured.

[0156] The package manufacturing process (step 1) is followed by the test process (step 2). Fig. 18 is a diagram showing the test process.

[0157] In the test process, test contactors 41 connected to a semiconductor device tester (not shown) are brought into contact with the external connection terminals 14 and the test terminals 16 exposed from the sealing resin 22. Then, the PT and the FT, which are carried out in separate steps in the related art, are implemented simultaneously.

[0158] That is to say, in the present embodiment, the test terminals 16 connected to the test chip terminals 13A can be used after the sealing resin 22 (insulating material) has been provided. Therefore, the test can be implemented using both the external connection terminals 14 and the test terminals 16. Thus, the PT, which is implemented before providing the sealing resin 22 in the related art, and the FT, which is implemented after providing the sealing resin 22 (i.e., a full test), can be implemented simultaneously. Accordingly, the test process can be simplified. Also, the external connection terminals 14 can be provided with a greater pitch than that for the PT implemented on the wafer. Therefore, it is possible to reduce an accuracy of the contactors connected to the external connection terminals 14 during the test. Thus, it is easier to make contact.

[0159] In the embodiment shown in Fig. 18, the contactors connected to the external connection terminals 14 and the test terminals 16 are shown as probe-type contactors, but contactors of a membrane type may be used.

[0160] When the test history recording part 33 is provided as in the wafer-level package 10K of the eleventh embodiment, shown in Fig. 13, the information obtained from the above-described test is stored in the test history recording part 33.

[0161] Further, when the wafer-level package 10B is used as an uncut semiconductor wafer, the cutting process (step 3) described later is omitted and the wafer-level package 10B is mounted on the mounting board.

[0162] The above-described package manufacturing process (step 1) and a test process (step 2) are followed by the cutting process (step 3). As shown in Fig. 19, in the cutting process, the outer region 18 is cut and removed by means of a dicing saw 39. Thus, individual-

ized semiconductor devices 40 are formed.

[0163] The cutting positions (dicing lines) of the dicing saw 39 are at the outer region 18 as shown by the dash-dot line shown in Fig. 3. Also, after the cutting process by the dicing saw 39, the size of the semiconductor device 40 viewed from above will be approximately equal to the size of the circuit region 12. That is to say, the semiconductor device 40 thus manufactured is a real-chip-size package.

[0164] Since the dicing saw 39 will cut along cutting regions in the outer region 18 and the components (in the present embodiment, the redistribution traces 15, the test terminals 16) provided in the outer region 18 are removed during the cutting process. According to the structure of the present embodiment, the manufacturing process can be simplified compared to the structure in which separate processes for removing the components 15, 16 are provided.

[0165] Also, since the redistribution traces 15 and the test terminals 16 will not remain on the individualized semiconductor devices 40, the semiconductor device 40 can be reduced in size. The presence of the redistribution traces 15 and the test terminals 16 will not alter the operating condition of the individualized semiconductor device 40.

[0166] The manufacturing method of the present embodiment has been described for the wafer-level package 10B. However, the wafer-level packages 10A, 10C to 10M of the first and third to thirteenth embodiments can also be manufactured using generally the same manufacturing method and the same effects can be achieved.

[0167] Also, with the wafer-level packages 10A, 10C to 10M of each embodiment, the components provided on the outer region 18 will be removed in the cutting process. Therefore, the presence of such components will not alter the operating condition of the individualized semiconductor device 40.

[0168] Further, the present invention is not limited to these embodiments, but variations and modifications may be made without departing from the scope of the present invention.

[0169] The present application is based on Japanese priority application No. 10-374804 filed on December 28, 1998, the entire contents of which are hereby incorporated by reference.

Claims

1. A wafer-level package (10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) characterized by comprising

a semiconductor wafer (11) having at least one semiconductor chip circuit forming region (12) each including a semiconductor chip circuit and a plurality of chip terminals (13, 13A, 13B), said

- chip terminals (13, 13A, 13B) including at least one test chip terminal (13A) and at least one non-test chip terminal (13B);
 at least one external connection terminal (14) electrically connected to said at least one non-test chip terminal (13B);
 at least one redistribution trace (15) provided on said semiconductor wafer (11), a first end of said redistribution trace (15) being connected to one of said test chip terminals (13A) and a second end of said redistribution trace (15) being extended out to a position offset from said one of said chip terminals (13, 13A, 13B);
 at least one testing member (16, 27, 33, 36) provided in an outer region (18) of said semiconductor chip circuit forming region (12), said second end of said redistribution trace (15) being connected to said at least one testing member (16, 27, 33, 36); and
 an insulating material (17, 19, 20) covering at least said redistribution trace (15), said at least one external connection terminal (14) and said at least one testing member (16, 27, 33, 36) being exposed from said insulating material (17, 19, 20).
2. The wafer-level package (10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) as claimed in claim 1, further comprising a sealing resin (22) provided on said insulating material (17, 19, 20) such that top parts of said external connection terminals (14) and said at least one testing member (16, 27, 33, 36) are exposed from said sealing resin (22).
 3. The wafer-level package (10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) as claimed in claim 1, characterised in that said at least one external connection terminal (14) and said at least one non-test terminal are electrically connected by an internal redistribution trace (15) in such a manner that said at least one external connection terminal (14) is provided at a position within said semiconductor chip circuit forming region (12) and offset from said at least one non-test chip terminal (13B).
 4. The wafer-level package (10D) as claimed in claim 1, characterised by further comprising an excessive power supply protection element provided in said outer region (18) and between said test chip terminal (13A) and said at least one testing member (16, 27, 33, 36).
 5. The wafer-level package (10A, 10B, 10C, 10D, 10E, 10F, 10H, 10I, 10J, 10M, 10N) as claimed in claim 1, characterised in that said at least one testing member (16, 27, 33, 36) includes at least one test terminal (16) corresponding to said least one semiconductor chip circuit forming region (12), respectively, said test terminal being provided in said outer region (18).
 6. The wafer-level package (10E) as claimed in claim 1, characterised in that said at least one testing member (16, 27, 33, 36) includes a plurality of test terminals (16) corresponding to a plurality of said semiconductor chip circuit forming regions (12), respectively, and at least one common line (25) connecting said test terminals (16), said test terminals (16) and said common line (25) being provided in said outer region (18).
 7. The wafer-level package (10E, 10G, 10L) as claimed in claim 1, further comprising at least one common line (25) provided in said outer region (18), a plurality of said redistribution traces (15) extending out of a plurality of said semiconductor chip circuit forming regions (12) being connected to said common line (25);
 characterised in that said at least one testing member (16, 27, 33, 36) includes a test pad (27) provided at a part of said common line (25) and exposed from said insulating material (17, 19, 20).
 8. The wafer-level package (10H) as claimed in claim 1, characterised by further comprising a plurality of units (28, 29) having different functions and provided within said semiconductor chip circuit forming region (12), a first end of said at least one redistribution trace (15) being connected to one of, or combination of, said units (28, 29) and a second end of said at least one redistribution trace (15) being connected to said at least one testing member (16, 27, 33, 36).
 9. The wafer-level package (10I) as claimed in claim 1, characterised by further comprising a test-purpose circuit (32) incorporated in said semiconductor chip circuit forming region (12), a first end of said at least one redistribution trace (15) being connected to said test-purpose circuit and a second end of said at least one redistribution trace (15) being connected to said at least one testing member (16, 27, 33, 36).
 10. The wafer-level package (10J) as claimed in claim 1, further comprising a test-purpose circuit (32A) provided in said outer region (18);
 characterised in that said at least one testing member (16, 27, 33, 36) is provided on the test-purpose circuit or on the redistribution trace (15) extending from the test-purpose circuit (32A).
 11. The wafer-level package (10K) as claimed in claim 1, characterised by further comprising

- a test history recording part (33) provided in said outer region (18) and connected to said second end of a plurality of said redistribution traces (15); and input/output terminals (34) for writing into/reading out from said test history recording part; said input/output terminals (34) being exposed from said insulating material (17, 19, 20).
12. The wafer-level package (10L) as claimed in claim 1, further comprising a common line (25) in said outer region (18); a plurality of said redistribution traces (15) extending out of a plurality of said semiconductor chip circuit forming region (12) being connected to said common line (25);
- characterised in that said at least one testing member (16, 27, 33, 36) includes a test supporting element (36) provided at a part of said common line (25) for testing said semiconductor chip circuit.
13. The wafer-level package (10M) as claimed in claim 1, characterised in that said at least one testing member (16, 27, 33, 36) includes a plurality of test terminals (16) provided with a predetermined rule in such a manner that said semiconductor wafer (11) can be identified from said positions of said test terminals.
14. A method of manufacturing a wafer-level package (10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) characterised by comprising the steps of:
- a) preparing a semiconductor wafer (11) having at least one semiconductor chip circuit forming region (12) each provided with a semiconductor chip circuit and a plurality of chip terminals (13, 13A, 13B); at least one of said chip terminals (13, 13A, 13B) being a test chip terminal (13A) and at least one being a non-test chip terminal (13B);
 - b) providing a redistribution layer including an insulating film (19, 20) having through holes on the semiconductor wafer (11) and an electrically conductive film formed on said insulating film (19, 20) said film (19, 20) being formed into redistribution traces (15) having a predetermined pattern;
 - c) providing external connection terminals (14) and at least one testing member (16, 27, 33, 36) on said redistribution layer; said at least one testing member (16, 27, 33, 36) being provided at an outer region (18) of said at least one semiconductor chip circuit forming region (12) and connected to said test chip terminal (13A) via at least one of said redistribution traces (15); and
 - d) testing said at least one semiconductor chip circuit using said at least one testing member (16, 27, 33, 36).
15. The method of manufacturing a wafer level package (10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) as claimed in claim 14, characterised by further comprising the step of
- e) providing a sealing resin (22) on said redistribution layer (19) in such a manner that top parts of said external connection terminals (14) and said at least one testing member (16, 27, 33, 36) are exposed from said sealing resin (22).
16. A method of manufacturing a semiconductor device using a wafer-level package (10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) characterised by comprising the steps of
- a) manufacturing a wafer-level package (10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) including a semiconductor wafer (11) having at least one semiconductor chip circuit forming region (12) each including a semiconductor chip circuit and a plurality of chip terminals (13, 13A, 13B); said chip terminals (13, 13A, 13B) including at least one test chip terminal (13A) and at least one non-test chip terminal (13B);
 - at least one external connection terminal (14) electrically connected to said at least one non-test chip terminal (13B);
 - at least one redistribution trace (15) provided on said semiconductor wafer (11); a first end of said redistribution trace (15) being connected to one of said test chip terminals (13A) and a second end of said redistribution trace (15) being extended out to a position offset from said one of said chip terminals (13, 13A, 13B); and
 - at least one testing member (16, 27, 33, 36) provided in an outer region (18) of said semiconductor chip circuit forming region (12); said second end of said redistribution trace (15) being connected to said at least one testing member (16, 27, 33, 36);
 - b) testing said at least one semiconductor chip circuit provided in said at least one semiconductor chip circuit forming region (12) using said at least one testing member (16, 27, 33, 36); and
 - c) after said step b), cutting said wafer-level package along said outer region (18) so as to manufacture at least one individualized semiconductor device.
17. The method of manufacturing a semiconductor de-

vice using a wafer-level package (10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10M, 10N) as claimed in claim 16, characterised in that in said step a), said external connection terminal (14) and said at least one testing member (16, 27, 33, 36) are manufactured simultaneously 5

18. The method of manufacturing a semiconductor device using a wafer-level package as claimed in claim 16, characterised in that in said step c), structures provided in said outer region (18), particularly said at least one testing member (16, 27, 33, 36), are removed simultaneously. 10

19. A wafer-level semiconductor device characterised by comprising 15

a semiconductor wafer (11) having chip circuit forming regions (12);
at least one testing member (16, 27, 33, 36) provided in an outer region (18) of the chip circuit forming regions (12); and
a line (15) provided on the semiconductor wafer (11) and connecting the at least one testing member (16, 27, 33, 36) and a test terminal provided in one of the chip circuit forming regions (12) 20 25

20. A semiconductor device characterised by comprising 30

a semiconductor chip;
a test terminal (13A) and a non-test terminal (13B) provided to the semiconductor chip, and
a line (15) which is connected to the test terminal (13A) and extends out of a circuit forming region (12) 35

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FIG.1

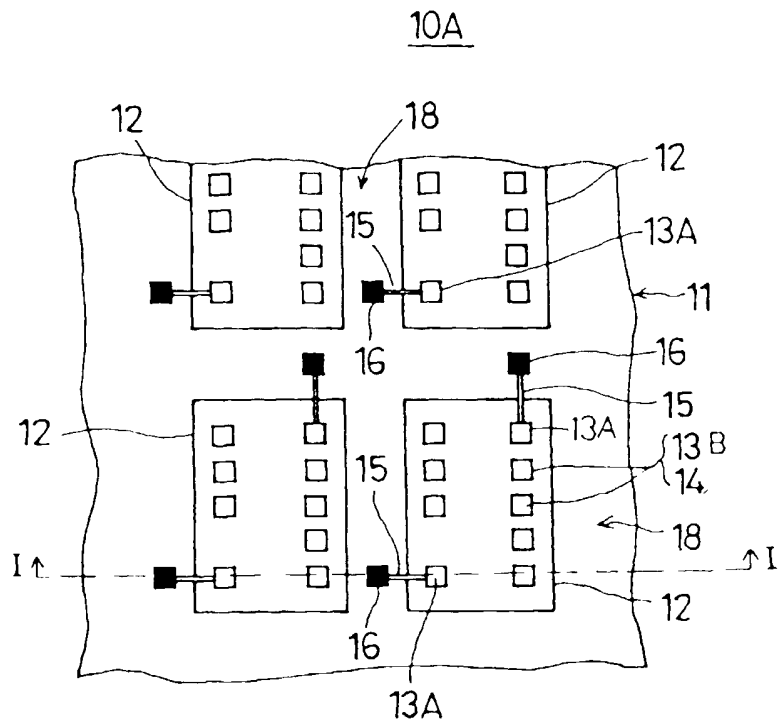


FIG.2

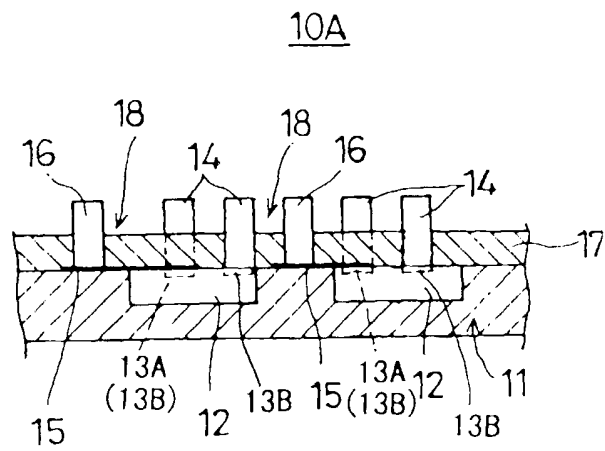


FIG.3

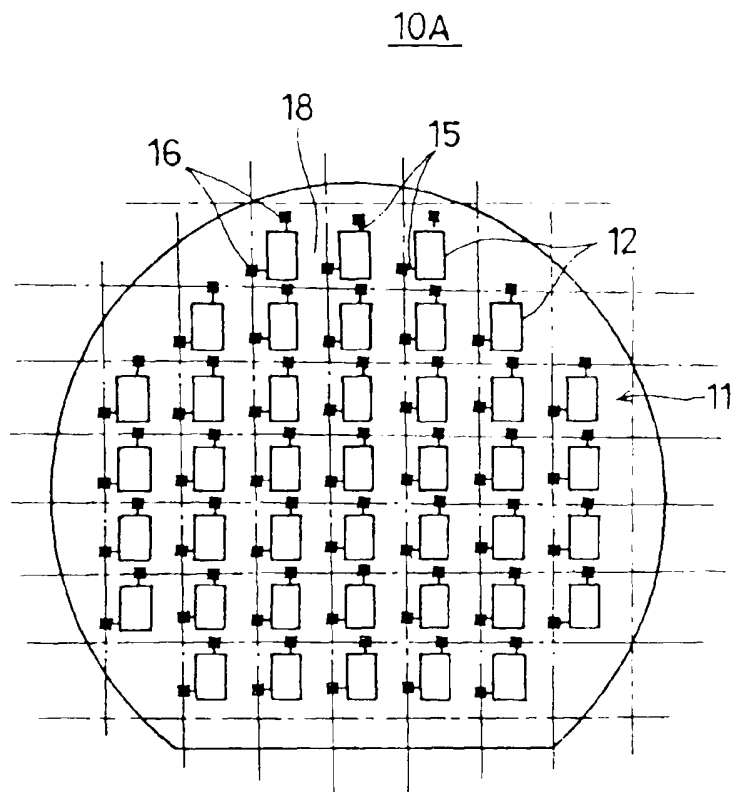


FIG.4

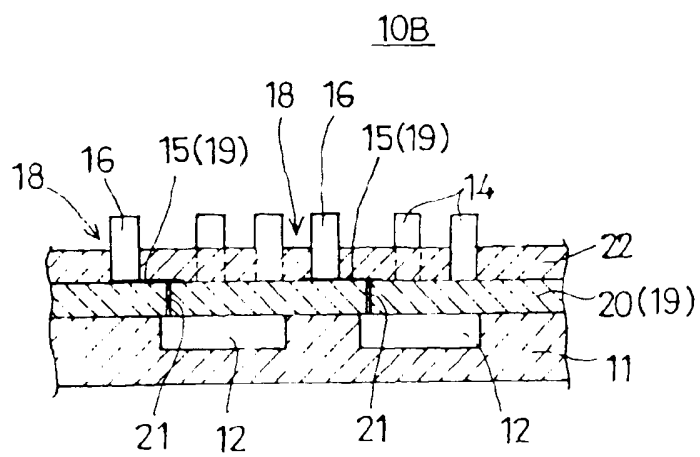


FIG.5

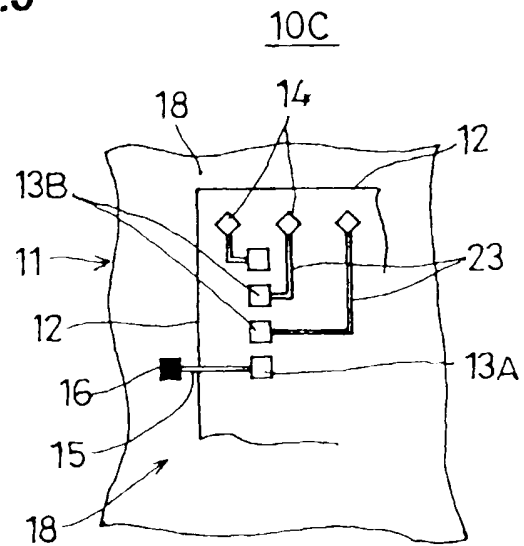


FIG.6

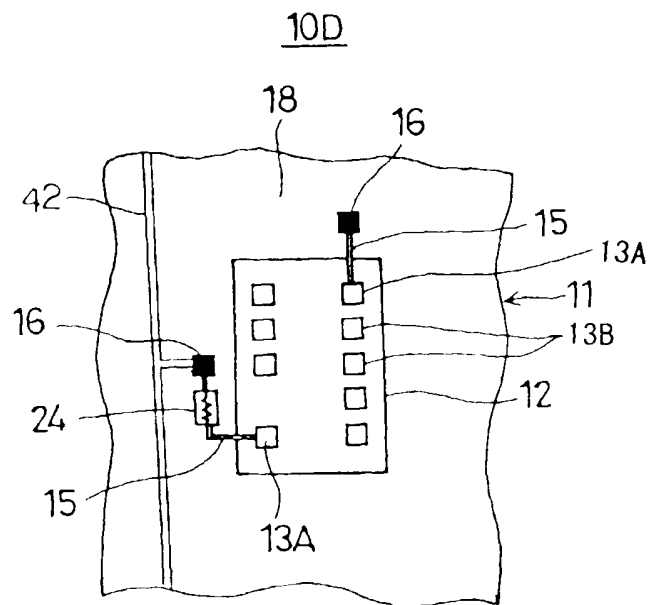


FIG.7

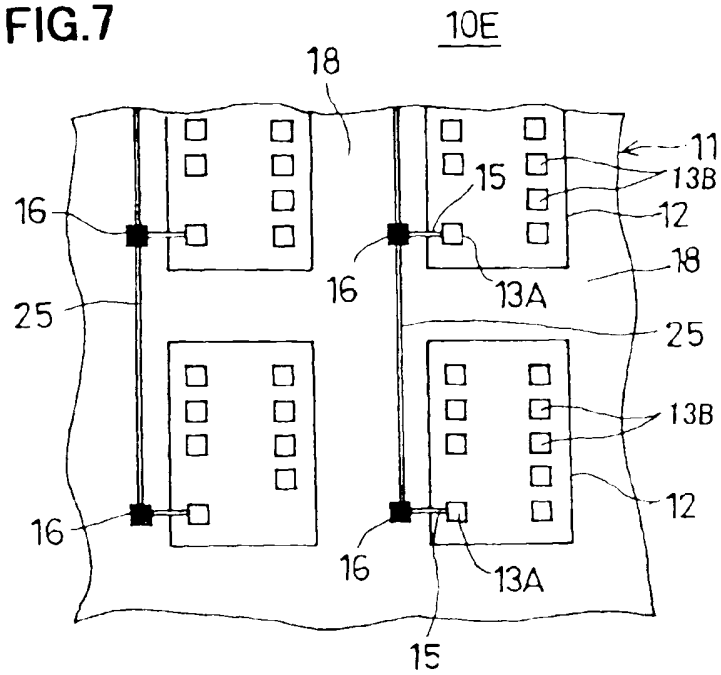


FIG.8

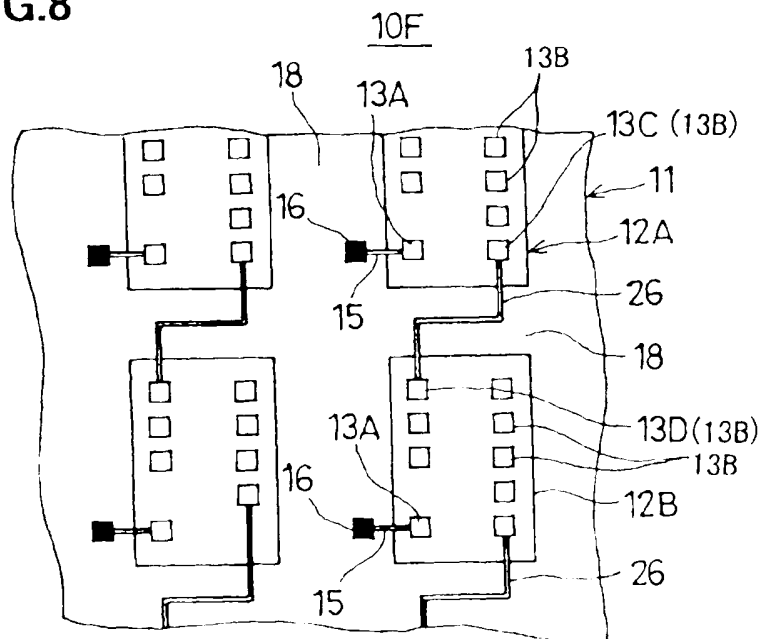


FIG.9

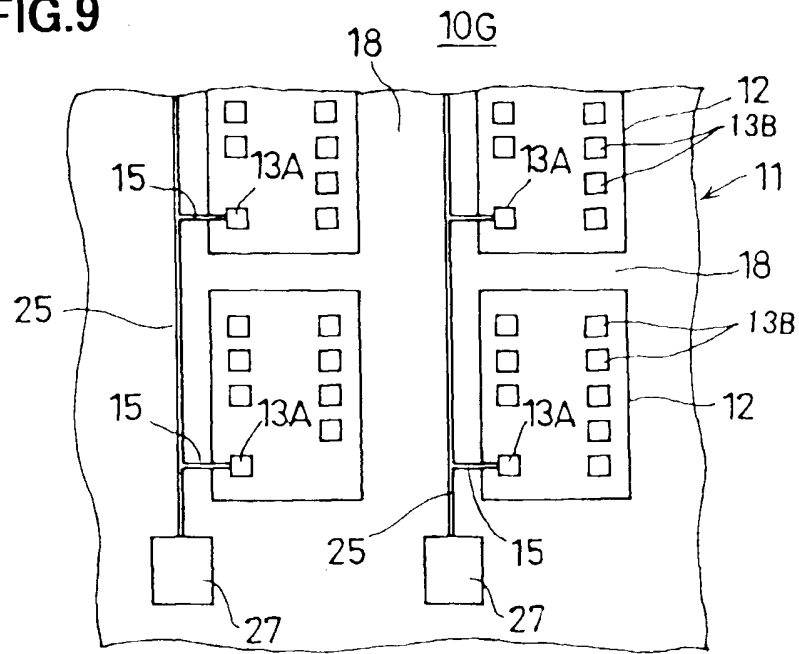


FIG.10

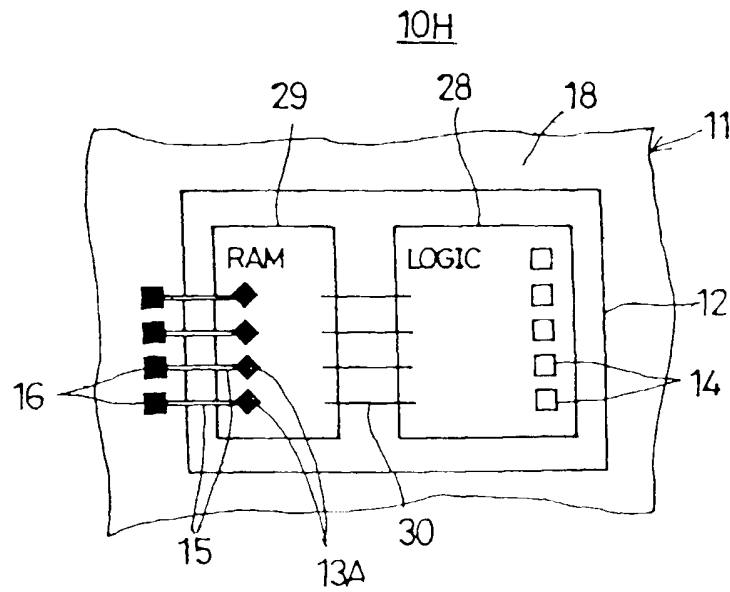


FIG.11

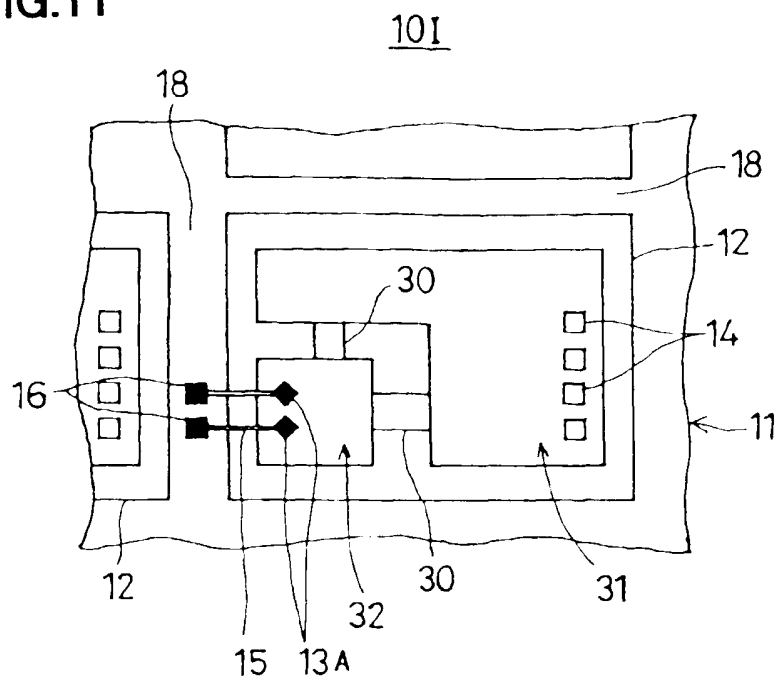


FIG.12

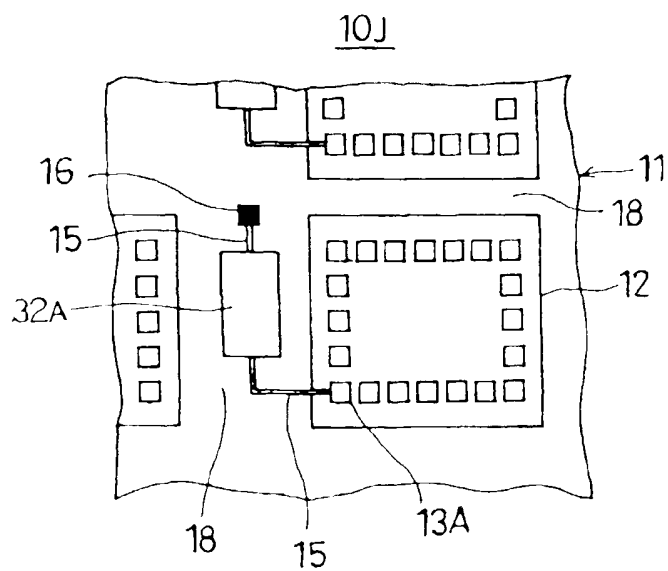


FIG.13

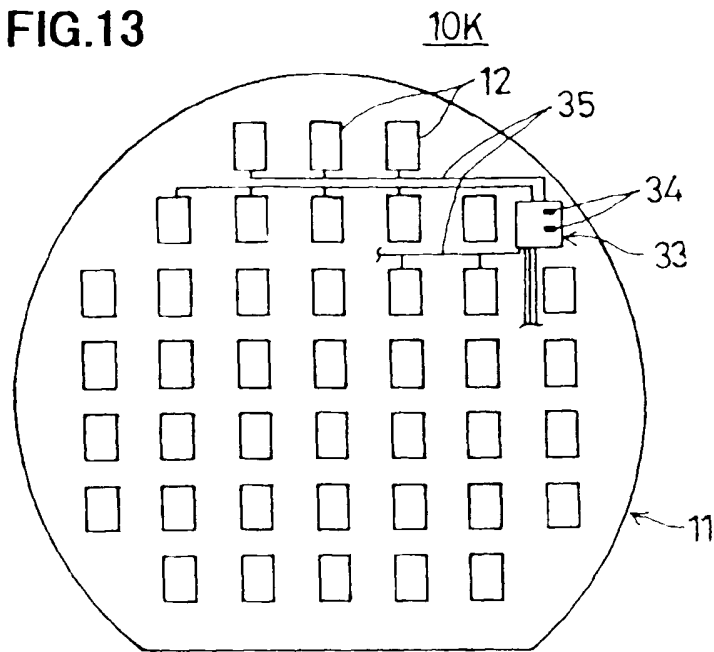


FIG.14

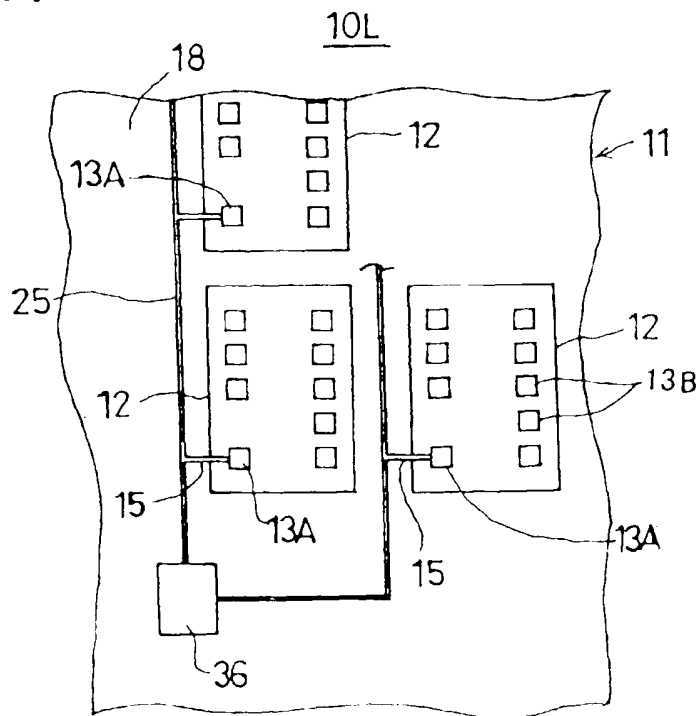


FIG.15

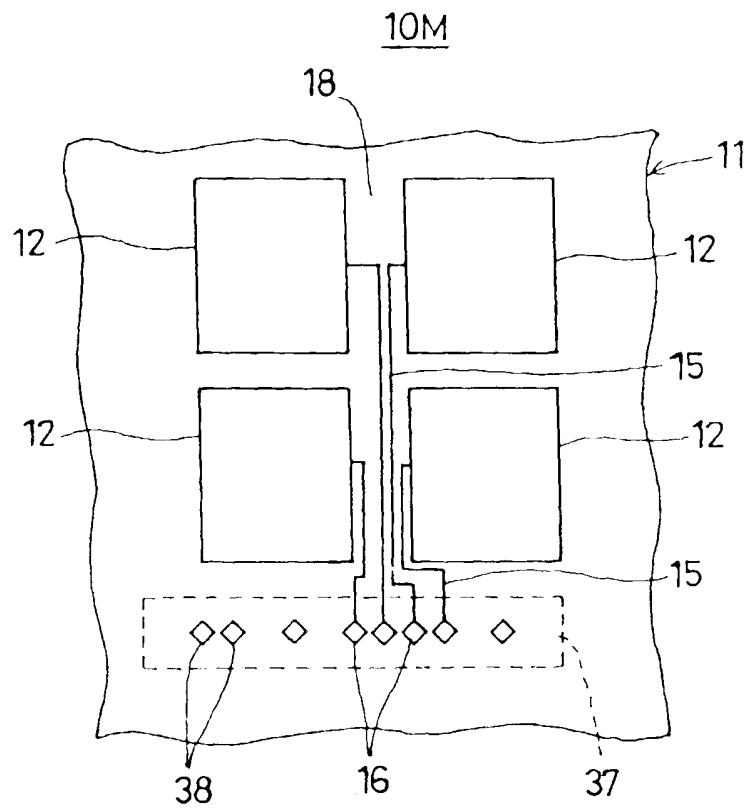


FIG.16

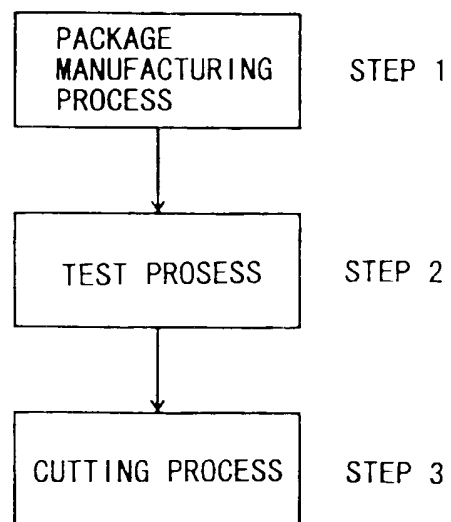


FIG.17A

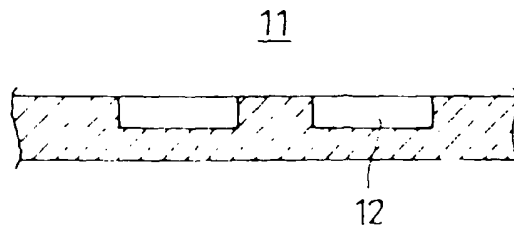


FIG.17B

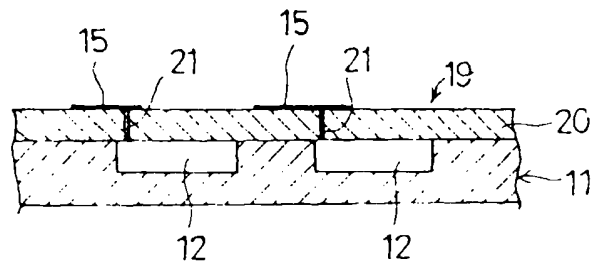


FIG.17C

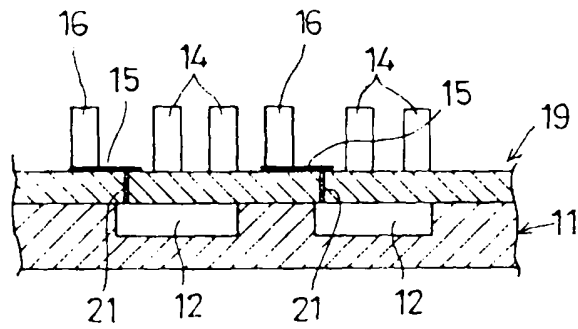


FIG.17D

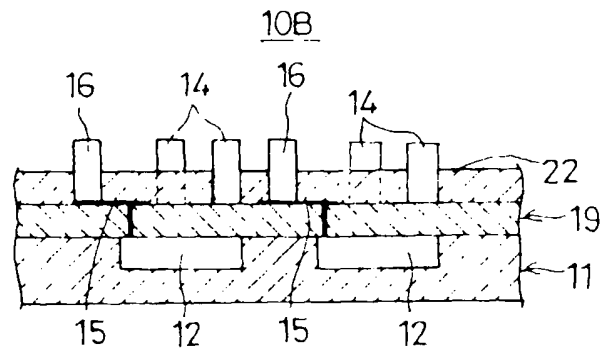


FIG.18

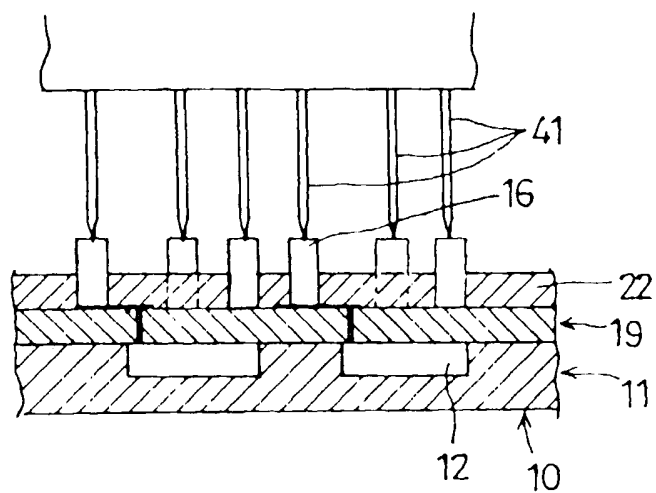


FIG.19

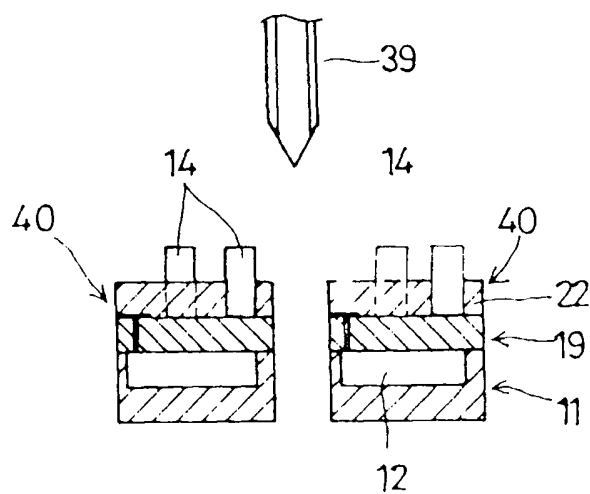


FIG.20

